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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/826,805	04/16/2004	Shih-Chang Shei	JCLA12240	1474
7590	06/21/2005		EXAMINER NADAV, ORI	
J.C. Patents, Inc. Suite 250 4 Venture Irvine, CA 92618			ART UNIT 2811	PAPER NUMBER

DATE MAILED: 06/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)	
	10/826,805	SHEI ET AL.	
	Examiner	Art Unit	
	ori nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED. (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10 June 2005.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-23 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-23 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The specification discloses a submount having a plurality of holes thereon and at least two LED chips on the submount, wherein at least one of the first patterned conductive film and the second patterned conductive film is commonly used by the LED chips. The submount is then diced to form grooves in separate mounts and LED chips. There is no support in the specification for a submount having a plurality of grooves thereon and at least two LED chips on the submount, wherein at least one of the first patterned conductive film and the second patterned conductive film is commonly used by the LED chips, as recited in claims 1 and 12.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claimed limitations of a submount having a plurality of grooves thereon and at least two LED chips on the submount, wherein at least one of the first patterned conductive film and the second patterned conductive film is commonly used by a plurality of the LED chip, as recited in claims 1 and 12, are unclear as to whether applicant claims an intermediate product, wherein at least two LED chips are formed on a submount and at least one of the first patterned conductive film and the second patterned conductive film is commonly used by a plurality of the LED chip, or a final product, wherein a submount having a plurality of grooves and one LED chip is formed on the submount.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 3-9, 12, 14-20 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murata (6,483,184) in view of Durocher et al. (6,614,103).

Regarding claims 1 and 12, Murata teaches in figure 1 and related text a chip package structure, comprising:

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a submount 18 having a first surface and a second surface opposite to the first surface, a plurality of grooves 18a on sidewalls of the submount;

a first patterned conductive film on a first part of the first surface 20, a first part of the second surface 26 and on a part of an inner wall of the grooves 28;

a second patterned conductive film on a second part of the first surface 20, a second part of the second surface 26 and a remaining part of the inner wall of the grooves 28; and

a chip 14 on the submount, wherein the chip has two electrodes electrically connecting with the first and second patterned conductive films 20, respectively.

Murata does not teach using the package for a flip-chip light emitting diode chip.

Durocher et al. teach in figure 12 using a package for at least two flip-chip light emitting diode chips 59.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use at least two flip-chip light emitting diode chips in Murata's package in order to use the device in an application which requires a flip-chip light emitting diode chips.

Note that a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

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Note further that a recitation in a preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

Regarding the claimed limitation of at least one of the first patterned conductive film and the second patterned conductive film is commonly used by LED chips, this feature is inherent in prior art's device, because at least one of the first patterned conductive film and the second patterned conductive film must be used by the plurality of the LED chips, since Durocher et al. teach in figure 12 at least two LED chips connected on the same substrate.

Regarding claims 3-9, 14-20 and 23, prior art teaches m is a number of the grooves that are on a first sidewall of the submount and n is a number of the grooves that are on a second sidewall of the submount,

wherein the first sidewall and the second sidewall are adjacent to each other,

wherein the first sidewall and the second sidewall are opposite to each other,

wherein m is equal and not equal to n,

wherein m is 1 and n is 1,

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wherein the grooves are on disposed on a sidewall at a corner of the submount,
and

wherein an angle formed between the sidewall and the bottom of the indentation
is an obtuse angle.

Regarding claims 10 and 21, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use bumps comprise a Sn-Pb alloy, a Sn-Au alloy or Au in prior art's device in order to improve the contact resistance of the device.

Regarding claim 12, Durocher et al. teach in figure 12 using a package for a flip-chip light emitting diode chip 59, wherein the light emitting diode chip 59 is formed inside an indentation of the submount. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form prior art's light emitting diode chip inside an indentation of the submount in order to improve the characteristics of the device.

Claims 2, 10-11, 13 and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murata and Durocher et al., as applied to claims 1 and 12 above, and further in view of Applicant Admitted Prior Art (AAPA).

Regarding claims 2, 10, 13 and 21, Murata and Durocher et al. teach substantially the entire claimed structure, as applied to claim 1 above, except two bumps disposed

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between the electrodes of the LED chip and the first patterned conductive film and the second patterned conductive film. AAPA teaches in figure 1B two bumps 106 disposed between the electrodes of the LED chip and the first patterned conductive film and the second patterned conductive film. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use two bumps disposed between the electrodes of the LED chip and the first patterned conductive film and the second patterned conductive film in prior art's device in order to reduce the resistance between the chip and the conductive films.

Regarding claims 11 and 22, AAPA teaches a submount comprises a material selected from the group consisting of aluminum nitride, boron nitride and zinc oxide.

Response to Arguments

Applicant argues that Murata does not equally disclose the same structure as recited in independent claims 1 and 12, because elements 20, 26 and 28 are not commonly used by other chips.

Applicant has no support for a first patterned conductive film and a second patterned conductive film (elements 20, 26 and 28) being commonly used by a plurality of the LED chips, as recited in claims 1 and 12. The specification discloses a submount having a plurality of holes thereon and at least two LED chips on the submount, wherein at least one of the first patterned conductive film and the second patterned conductive

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film is commonly used by a plurality of the LED chip. The submount is then diced to form grooves in separate mounts and LED chips. There is no support in the specification for a submount having a plurality of grooves thereon and at least two LED chips on the submount, wherein at least one of the first patterned conductive film and the second patterned conductive film is commonly used by a plurality of the LED chip, as recited in claims 1 and 12. In any event, at least one of the first patterned conductive film and the second patterned conductive film is commonly used by LED chips, this feature is inherent in prior art's device, because at least one of the first patterned conductive film and the second patterned conductive film must be used by the plurality of the LED chips, since Durocher et al. teach in figure 12 at least two LED chips connected on the same substrate.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

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Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(571) 272-1660**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

A handwritten signature in black ink, appearing to read 'Ori Nadav', is positioned above the printed name.

O.N.
6/17/05

ORI NADAV
PRIMARY EXAMINER
TECHNOLOGY CENTER 2800